# SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY MODULE

**MODEL NO.: HY-1602F-801**  
**DATE:** AUG. 22. 2003

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<tr>
<th>Approved</th>
<th>Checked</th>
<th>Department</th>
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**CUSTOMER:**  
**MODEL NO.:**  
**DATE:**

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</table>
CONTENTS

I. General Specification--------------------------------------------------------(3-6)

II. The Characteristics and Reliability Test---------------------------------(7-8)

III. The LCD Measuring Method and Equipment-------------------------------(9-11)

IV. Standard Specifications for Product Quality----------------------------- (12-13)

V. Instruction System and Description of Details----------------------------- (19-26)
I. General Specifications

1. General

The AV-DISPLAY dot matrix LCD module consists of the liquid crystal display C-MOS driver and C-MOS LSI controller. The module utilizes 5*7 dot matrix characters to provide full alphanumeric capability. All control, refresh, and display functions are executed by a dedicated on-board controller. The module is capable of displaying the full 160-character JIS font set. Data interfacing is via the 4-bit or 8-bit bi-directional data bus by using simple control commands. The data can be selectively written to the data register.

2. Features

A. Built-In Controller LSI.
B. 5*7 Dot Matrix With Cursor.
C. Micro-Processor Compatible Data-Bus Interface (4-Bit Or 8-Bit).
D. Character Generator ROM Built-In
   5*8 Dot: ---------208 Character Fonts
   5*10 Dot: ---------32 Character Fonts
E. Character Generator RAM---------Customer Rewritable
   5*8 Font:8 Characters
F. Powerful Control Command
   (1) Display Clear
   (2) Return Home
   (3) Cursor Preset
   (4) Cursor On/Off Or Cursor Blinking
   (5) Cursor Display Shift
   (6) Display Shift
   (7) Display On/Off Control
   (8) Display Data Read/Write
G. Low power consumption 5.0v power supply
H. Attaching drawing and general description.

HY-1602F-801

16x2 CHARACTERS
1/16DUTY, 1/5BIAS

DATE: AUG 22, 2003

TECHNICAL SPECIFICATION

LCM

HY-1602F-801

Page 4 of 26
4. Timing Characteristics:

Write Operation and Read Operation

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Cycle Time</td>
<td>T_{CYCLE}</td>
<td>500</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
<tr>
<td>Enable Pulse Width</td>
<td>P_{WEH}</td>
<td>220</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
<tr>
<td>Enable Rise &amp; Fall Time</td>
<td>T_{ER,T_{EF}}</td>
<td>--</td>
<td>--</td>
<td>25</td>
<td>nS</td>
</tr>
<tr>
<td>Address Set-Up Time</td>
<td>T_{AS}</td>
<td>40</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>T_{AH}</td>
<td>10</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
<tr>
<td>Data Set-Up Time</td>
<td>T_{DSW}</td>
<td>60</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>T_{H}</td>
<td>10</td>
<td>--</td>
<td>--</td>
<td>nS</td>
</tr>
</tbody>
</table>
5. Write Operation:

- RS
- R/W
- E
- DB0—DB7

Read Operation

- RS
- R/W
- E
- DB0—DB7

Diagram illustrating the timing and signal flow for both write and read operations.
### The Characteristics and The Reliability Test

#### 1. Electro-Optic Characteristics:

<table>
<thead>
<tr>
<th>Condition: TEMP=(21 ± 3)°C</th>
<th>HUM=(70 ± 5)%RH</th>
</tr>
</thead>
</table>

- **V\text{DD}:** 5.0V
- **F\text{OSC}:** 270KHZ

#### Table

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Operating Voltage</td>
<td>\text{Vop}</td>
<td>5.0</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2. Current Consumption</td>
<td>\text{Is}</td>
<td>1.30</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>3. Response Time</td>
<td>\text{Ton}</td>
<td>150</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>\text{Toff}</td>
<td>120</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>4. Contrast</td>
<td>\text{CR}</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5. Viewing Angle (CR \geq 3.0)</td>
<td>\text{01}</td>
<td>15</td>
<td></td>
<td></td>
<td>Deg.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>\text{02}</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>\text{03}</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>\text{04}</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6. Threshold Voltage</td>
<td>\text{Vth}</td>
<td>1.14</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>7. Backlight Current Consumption</td>
<td>\text{LED}</td>
<td>30</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>No</td>
<td>Items</td>
<td>Test Condition</td>
<td>Test Result</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----</td>
<td>----------------------</td>
<td>--------------------------------</td>
<td>-------------</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>High Temp Storage</td>
<td>Temp: 70°C ± 2°C Time: 96h Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Low Temp Storage</td>
<td>Temp: -20°C ± 3°C Time: 96h Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>High Temp Static drive</td>
<td>Temp: 50°C ± 2°C Vop: 5V Time: 96h Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Low Temp Static drive</td>
<td>Temp: 0°C ± 3°C Vop: 5V Time: 96h Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>High Temp High Hum Storage</td>
<td>Temp: 40°C ± 2°C Hum: 95%Rh Time: 96h Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Thermal Shock</td>
<td>Temp: 5 Cycles Restore: 24h</td>
<td>Passed</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
III. The LCD Measuring Method and Equipment

1. Current Consumption Measuring
   (1) Equipment

   - DC Power Supply
   - Waveform Generator: F=64HZ

   (2) Condition
   Operating Frequency: 64HZ
   Operating Voltage (RMS): Selected Voltage

2. Threshold Voltage and Response Time Measuring
   (1) Equipment

   - Oscilloscope
   - Waveform Generator
   - 30°
(2) Definition
A. Threshold Voltage \((V_{th})\)

![Graph showing the relationship between drive voltage and brightness, with thresholds for 100%, 80%, and 50% brightness.]

B. Response Time

![Graph showing the relationship between time and percentage of on and off states, with time constants \(T_r\) and \(T_d\).]
3. Contrast Measuring

(1) Equipment

![Diagram of equipment setup]

(2) Definition:

A. Viewing Angle:

- $\theta_1$ and $Y_{12h}$,
- $\Phi = 90^\circ$
- $\theta_2$ and $6h$, $\Phi = 270^\circ$
- $\theta_3$ and $X_{3h}$, $\Phi = 0^\circ$
- $\theta_4$ and $9h$, $\Phi = 180^\circ$

B. Contrast Ratio (Positive)

$$CR = \frac{\text{Brightness of non-selected wave-form}}{\text{Brightness of selected wave-form}}$$
IVA. Standard Specifications for Product Quality

1. Manner of Test:
   1.1. The Test Must Be Under 40w Flourescent Light, And The Distance Of View Must Be At 30cm.
   1.2. The Test Direction Is Based On Around 15° - 45° Of Vertical Line.

2. Definition Of Defects
   2.1 Major Defects
   A: Non-Display
   B: Segment Missing
   C: Over Current
   D: Segment Short
   E: Sealant Dishardexn
   F: Wrong Polarizer Direction

2.2 Interface Circuit and Drive Programme on LCM of character series.
   A. Interface circuit:

   ![Interface Circuit Diagram]

   0—20k

   B. Drive programme for testing LCM of character series.
ORG 0000H
AJMP MAIN

ORG 0300H
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,
DB 58H,58H,58H,58H,58H,58H,58H,

ORG 0350H
DB 2AH,59H,55H,53H,55H,4EH,47H,2AH,
DB 45H,4CH,45H,43H,2EH,4CH,54H,44H,
DB 2AH,44H,4FH,54H,2AH,4DH,41H,54H,
DB 52H,49H,58H,2AH,4CH,43H,44H,2AH,
DB 4BH,65H,5AH,6FH,6EH,48H,75H,69H,
DB 2AH,59H,55H,53H,55H,4EH,47H,2AH,
DB 45H,4CH,45H,43H,2EH,4CH,54H,44H,
DB 2AH,44H,4FH,54H,2AH,4DH,41H,54H,
DB 52H,49H,58H,2AH,4CH,43H,44H,2AH,
DB 4BH,65H,5AH,6FH,6EH,48H,75H,69H,
DB 2AH,2AH,2AH,2AH,2AH,2AH,2AH,2AH,
DB 44H,4FH,54H,20H,4DH,41H,54H,52H,
DB 49H,58H,20H,4CH,49H,51H,55H,49H,
DB 44H,20H,43H,52H,59H,53H,54H,41H,
DB 4CH,20H,44H,49H,53H,50H,4CH,41H,
DB 59H,20H,4DH,4FH,55H,44H,4CH,45H,
DB 2AH,2AH,2AH,2AH,2AH,2AH,2AH,2AH,
DB 2AH,2AH,2AH,2AH,2AH,2AH,2AH,2AH,
DB 54H,4DH,0B0H,44H,4DH,43H,34H,30H,
DB 32H,2AH,2AH,2AH,2AH,2AH,2AH,2AH,
DB 2AH,2AH,2AH,2AH,2AH,2AH,2AH,2AH,
DB 2AH,2AH,2AH,2AH,2AH,2AH,2AH,2AH,

MAIN:
MOV SP, #60H ;Initial for the first display
MOV P1, #38H ;set function
LCALL WINST
MOV P1, #0EH ;set display on/off control
LCALL WINST
MOV P1, #06H ;set Entry mode
LCALL WINST
MOV P1, #01H ;clear display,write code 20h into all DDRAM
LCALL WINST
LCALL DELAY1

MOV DPTR, #0300H
MOV R0, #28H ;Set Pointer
MOV R2, #00H
MOV A, #00H
MOV P1, #80H ;set DDRAM address 0000h
LCALL WINST
LOOP1:
MOVC A, @A+DPTR
MOV P1, A
LCALL WDATA
INC R2
MOV A, R2
DJNZ R0, LOOP1
MOV DPTR, #0328H
MOV R0, #28H
MOV R2, #00H

MOV DPTR, #0328H
MOV R0, #28H
MOV R2, #00H
MOV A, #00H
MOV P1, #0C0H
LCALL WINST

LOOP2:
    MOVC A, @A+DPTR
    MOV P1, A
    LCALL WDATA
    INC R2
    MOV A, R2
    DJNZ R0, LOOP2 ;The first display is over
    LCALL DELAY2 ;paused about 5ms

    MOV SP, #60H ;initial for the second display
    MOV P1, #38H
    LCALL WINST
    MOV P1, #0EH
    LCALL WINST
    MOV P1, #06H
    LCALL WINST
    MOV P1, #01H
    LCALL WINST
    LCALL DELAY1

    MOV DPTR, #0350H ;ready for the first line display
    MOV R0, #28H
    MOV R2, #00H
    MOV A, #00H
    MOV P1, #80H
    LCALL WINST

LOOP3:
    MOVC A, @A+DPTR
    MOV P1, A
    LCALL WDATA
INC  R2
MOV  A, R2
DJNZ  R0, LOOP3  ;THE first line display is over

MOV  DPTR, #0378H  ;ready for the second line display
MOV  R0, #28H
MOV  R2, #00H
MOV  A, #00H
MOV  P1, #0C0H
LCALL  WINST
LOOP4:
  MOV  A, @A+DPTR
  MOV  P1, A
  LCALL  WDATA
INC  R2
MOV  A, R2
DJNZ  R0, LOOP4  ;main program is end upto here
LOOP5:
  LCALL  DELAY2
  AJMP  MAIN

WINST:
  CLR  P3.0  ;write to instruction register
  CLR  P3.2
  SETB  P3.1
  LCALL  DELAY1
  CLR  P3.1
  LCALL  DELAY1
  RET

WDATA:
  CLR  P3.2  ;write to data register
  SETB  P3.0
  SETB  P3.1
LCALL  DELAY1
CLR    P3.1
LCALL  DELAY1
RET

DELAY1:
    MOV    50H, #08H     ;delay 1648 us
ADDR1:  PUSH   50H
ADDR2:  PUSH   50H
ADDR3:  PUSH   50H
ADDR4:  DJNZ   50H, ADDR4
         POP     50H
         DJNZ   50H, ADDR3
         POP     50H
         DJNZ   50H, ADDR2
         POP     50H
         DJNZ   50H, ADDR1
         RET

DELAY2:
    MOV     R0, #0CCH
    MOV     R2, #66H
ADDR5:
    LCALL  DELAY1         ;delay ccH X 1648us
DJNZ    R0, ADDR5
ADDR6:
    LCALL  DELAY1         ;delay 66H X 1648us   total 5.05ms
DJNZ    R2, ADDR6
RET

END
### 3. Inspection Item and Standards

<table>
<thead>
<tr>
<th>Item</th>
<th>The Standard Of Quality Inspection</th>
<th>Checking Manner</th>
<th>Quality Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame</td>
<td>Smooth and even surface, no crack, no scratch, no rusty, and not be wrenched out of shape. The range between convex and concave is: $d \leq 0.35\text{mm}$, and the frame must be connected to the ground.</td>
<td>Checking With Eyes And Using Vernier Caliper, Multimeter</td>
<td>100%</td>
</tr>
<tr>
<td>LCD</td>
<td>The major defects would be reject. No scratch and no dusty on the LCD glass surface. $d \leq 0.15\text{mm}$, $n \leq 2$ diameter of bubble: $d \leq 0.5$, $n \leq 2$ damaged size of polarizer: $d \leq 0.15\text{mm}$, $n \leq 2$.</td>
<td>Check It When Displaying</td>
<td>100%</td>
</tr>
<tr>
<td>The Relative Position of LCD and Frame</td>
<td>The sealant mouth of the LCD must be at the same side with the frame’s.</td>
<td>Checking With Eyes</td>
<td>100%</td>
</tr>
<tr>
<td>The Relative Position of PCB Panel and Frame</td>
<td>The frame installing direction must be correct. The twisted angle of the pin is from $45^\circ$ to $60^\circ$, the pin is vertical to PCB panel and it must be in the middle position of the installing holes.</td>
<td>Checking With Eyes</td>
<td>100%</td>
</tr>
</tbody>
</table>
| Function Test | 1. The major defects must be reject.  
2. Test flow chart (see attached chart)  
3. Background changes evenly and no disorderly displaying phenomenon.  
4. Display no shortage. | Check It When Displaying | 100% |

Note: $D \sim$ Diameter  \quad $N \sim$ Quantity  \quad Unit:mm
V. Instruction System and Description of Details

1. Instruction System

Only two SPLC780A OR S6A0069X01-C0CX registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface form SPLC780A OR S6A0069X01-C0CX internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICS. SPLC780A OR S6A0069X01-C0CX internal operation is determined by signals sent from the MPU. These signals include register selection signal (RS), read/write signals (R/W) and data bus signals (DB0—DB7), and are called instructions, here. Table 1 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate SPLC780A OR S6A0069X01-C0CX functions such as display format, data length, etc.

(2) Give internal RAM addresses.

(3) Perform data transfer with internal RAM.

(4) Others.

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by –1) of SPLC780A OR S6A0069X01-C0CX internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency. For an explanation of the shift function in its relation to display, . When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to “1” while an instruction is being executed, check to make sure it is on “1” before sending an instruction from the MPU.

Note 1

Make sure the SPLC780A OR S6A0069X01-C0CX is not in the busy state (BF=0) before sending the instruction from the MPU to the SPLC780A OR S6A0069X01-C0CX. If the instruction is sent without checking the busy flag the time between first and next instructions is much longer than the instruction time.

See Table 1 for a list of each instruction execution time.

Note 2

After executing instruction of writing data to CG/DD RAM or reading data from CG/
DD RAM, RAM address counter is automatically incremented by 1 (or decremented by 1). In this case, this shift is executed after Busy flag is set to “Low”. \( T_{ADD} \) is stipulated the time from the fall edge of busy flag to the end of address counter’s renewal.

### Busy signal (BD)

<table>
<thead>
<tr>
<th>Address counter(DB - DB)</th>
<th>A</th>
<th>A+ 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{ADD} = \frac{1.5}{f_{CP} \text{ or } f_{OSC}} ) (s)</td>
<td>( t_{ADD} ) depends on the operating frequency</td>
<td></td>
</tr>
</tbody>
</table>

### Table 1 Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
<th>Execution time (when Fosc is 250 KHz)</th>
<th>Execution time (when Fosc is 160 KHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear display</td>
<td>0 0 0 0 0 0 0 0 0 0 1</td>
<td>Clears all display and returns the cursor to home position (Address 0)</td>
<td>82us~1.64ms</td>
<td>120us~4.9ms</td>
</tr>
<tr>
<td>Return home</td>
<td>0 0 0 0 0 0 0 0 0 0 1</td>
<td>* Reverts the display and returns the cursor to the home position (Address 0) Also returns the display being shifted to the original position. DRAM contents remain unchanged</td>
<td>40us~1.6ms</td>
<td>120us~4.8ms</td>
</tr>
<tr>
<td>Entry mode set</td>
<td>0 0 0 0 0 0 0 0 1 I/D S</td>
<td>* Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Display ON/OFF control</td>
<td>0 0 0 0 0 0 0 1 D C B</td>
<td>* Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B)</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Cursor and display shift</td>
<td>0 0 0 0 0 0 1 S/C R/L</td>
<td>* * Moves the cursor and shifts the display without changing DD RAM contents.</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Function set</td>
<td>0 0 0 0 0 1 DL N F</td>
<td>* * Sets interface data length (DL), number of display lines (L), and character font (F)</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Set CG RAM address</td>
<td>0 0 0 1 ACG</td>
<td>* * Sets interface data length (DL), number of display lines (L), and character font (F).</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Set DD RAM address</td>
<td>0 0 1 ADD</td>
<td>* * Sets the DD address. DD RAM data is sent and received after this setting.</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Read busy flag &amp; address</td>
<td>0 1 BF AC</td>
<td>* * Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.</td>
<td>1us</td>
<td>1us</td>
</tr>
<tr>
<td>Write data to CG or DD RAM</td>
<td>1 0 Write Data</td>
<td>* * Writes data into DD RAM or CG RAM.</td>
<td>40us</td>
<td>120us</td>
</tr>
<tr>
<td>Read data to CG or DD RAM</td>
<td>1 1 Read Data</td>
<td>* * Reads data from DD RAM or CG RAM.</td>
<td>40us</td>
<td>120us</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/D=1: Increment (+1) I/D=0: Decrement (-1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S =1: Accompanies display shift</td>
</tr>
<tr>
<td>S/C=1: Display shift S/C=0:Cursor move</td>
</tr>
<tr>
<td>R/L=0: Shift to left</td>
</tr>
<tr>
<td>R/L=0: Shift to right</td>
</tr>
<tr>
<td>DL = 8 bits</td>
</tr>
<tr>
<td>DL = 4 bits</td>
</tr>
<tr>
<td>F = 1: 5x10 dots</td>
</tr>
<tr>
<td>F = 0: 5x7 dots</td>
</tr>
<tr>
<td>BF = 1: Internally operating</td>
</tr>
<tr>
<td>BF = 0: Can accept instruction</td>
</tr>
</tbody>
</table>

* No effect

Notes 1: Applied to models driven by 1/8 duty or 1/11 duty.
2: Applied to models driven by 1/16 duty.

### 2. Description of details

1. **Clear display**

   RS R/W DB7

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clears all display and returns the cursor to home position (Address 0)</td>
</tr>
</tbody>
</table>

   Notes:

   - **CG RAM**: Character generator RAM
   - **ADD**: DD RAM address
   - **AC**: Address counter used for both DD and CG RAM

   Execution time changes when frequency changes. (Example)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Execution time</th>
</tr>
</thead>
<tbody>
<tr>
<td>270 kHz</td>
<td>200us x 270 = 37us</td>
</tr>
</tbody>
</table>

   **Remarks**:

   - When Fosc is 270kHz:
   - 250us x 270 = 37us
(2) Return home

RS   R/ W   DB7  ----------------------------------------------------------------------DB0
Code 0 0 0 0 0 0 0 0 0 0 0 0 1

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

RS   R/ W   DB7  ----------------------------------------------------------------------DB0
Code 0 0 0 0 0 0 0 0 0 0 0 0 1 I/D  S

I/D: Increments (I/D = 1) or decrement s (I/D) the DD RAM address by 1 when a character code is written into or read from the DD RAM . The cursor blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM it does it shift when S = 0.

(4) Display ON/OFF control

RS   R/ W   DB7  ----------------------------------------------------------------------DB0
Code 0 0 0 0 0 0 0 0 1  D  C  B

D: The display is ON when D = 1 and OFF when D = 0. when off due to D = 0, display Data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the Cursor disappears, the function of I/D, etc. does not change during display data write.

The cursor is displayed using 5 dots in the 8th line when the 5x7 dot character font
Is selected and 5 dots in the 11th line when the 5x10 dot character font is selected.

**B:** The character indicated by the cursor blink when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when fcp or fosc = 250Khz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. 409.6x250/270 = 379.2ms when fcp = 270kHz).

---

(a) Cursor Display Example  
(b) Blink Display Example

---

(5) Cursor or display shift

```
Code 0 0 0 0 0 1 S/c R/l * *
```

*No effect

Shifts Cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-lines display, the cursor moves to the 2nd line when its passes the 40th digit of the 1st line. Notice that the 1st and 2nd line display will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

**S/C R/L**

0 0 Shifts the cursor position to the left. (AC is decremented by one.)
0 1 Shifts the cursor position to the right. (AC is decremented by one.)
1 0 Shifts the entire display to the left. The cursor follows the display shift.
2 1 Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift.

(6) Function set

```
Code 0 0 0 0 1 DL N F *
```

*No effect

**DL:** Sets interface data length. Data is sent or received in 8 bit lengths (DB7~DB0) when DL = 1 and in 4 bit lengths (DB7~DB4) when DL = 0. When the 4 bit length is selected.
Data must be sent or received twice.

**N**: Sets number of display lines

**F**: Sets character font.

(Note) Perform the function at the head of the program before executing all instruction (expect “Busy flag/address read”). From this point, the function set instruction cannot be executed unless the interface data length is changed.

<table>
<thead>
<tr>
<th>N</th>
<th>F</th>
<th>No. of display lines</th>
<th>Character font</th>
<th>Duty factor</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>5x7 dots</td>
<td>1/8</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>5x10 dots</td>
<td>1/11</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>*</td>
<td>2</td>
<td>5x7 dots</td>
<td>1/16</td>
<td>Cannot display 2 lines with 5x10 dot character font.</td>
</tr>
</tbody>
</table>

*No effect*

(7) Set CG RAM address

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0001AA A A A A</td>
</tr>
</tbody>
</table>

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>001 A A A A A A A A</td>
</tr>
</tbody>
</table>

Sets the DD RAM address into the address counter in binary AAAAAAAA. Data is then written or read from the MPU for the DD RAM. However, When N = 0 (1-line display), AAAAAAA is “00” ~ “4F” (hexadecimal). When N = 1 (2-line display), AAAAAAAA is “00” ~ “27” (hexadecimal) for the first line, and “40” ~ “67” (hexadecimal) for the second line.

(9) Read busy flag & address

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>BF</td>
<td>01AA A A A A A A</td>
</tr>
</tbody>
</table>

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to “0”. Check the BF status before the next write operation. At the same time, the value of the address counter expressed in binary AAAAAAAA is read out. The address counter is used by both CG
and DD RAM address, and its value is determined by the previous instruction. Address contents are the same as in terms (7) and (8).

(10) Write data to CG or DD RAM

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>D</td>
<td>D</td>
</tr>
</tbody>
</table>

←Higher Order Bits

| Lower Order Bits→

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>D</td>
<td>D</td>
</tr>
</tbody>
</table>

←Higher Order Bits

| Lower Order Bits→

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don’t, the first read data will be invalidated. When serially executing the “read” instruction, the next address data is normally read from the second read. The “address set” instruction need not be executed just before the “read” instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM’s address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after “write” instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if “read” instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the “read” instruction from the second time the “read” instruction is serial.
3. Precaution on programming

(1) Instruction of function set

Perform the function at the head of program that accesses SPLC780A OR S6A0069X01-C0CX before executing all instructions, and not change the data of the instruction Register in the program. The data of function register can be changed by the program as follow;

a. • Changing of DL (Data Length)
   • when DL is changed from 8-bit length mode.
   • when DL is changed from 4-bit length mode.

b. • Changing of N (Column Number)
   • Perform the instruction of function set after executing instruction of display clear or display off.

In this case, sequence of AC and DD RAM must be changed. Thus, rewrite the address set register after that.

c. • Changing of F (Font)
   • There is no problem in this case, but for dual-line display, the font mode of 5x11 cannot be selected (this mode is forbidden by hardware).

When N of F is changed, power supply voltage for LCD must be changed. If not Changed, crosstalk will appear, or contrast will be poor.

(2) Busy flag check

SPLC780A OR KS0066 is produced in the CMOS process, therefore internal executing time is long.

Standard time is 40us~1.6ms. (This varies by instruction).

When the high speed MPU controls it, check the busy flag before performing Instruction or reading data.

While internal operation is active, Enable signal is not accepted. (Enable signal at Reading status register for checking busy flag is accepted) Busy flag signal is output through DB7, as shown in Table 3, when RS = “0”, R/W = “1 “, and Enable = “1”

(3) Input of unidentified instruction code

Undefined instruction code of SPLC780A OR S6A0069X01-C0CX is only as follows;

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7~DB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0~</td>
</tr>
</tbody>
</table>

(Others are included to defined instruction)

When the undefined instruction code is loaded to SPLC780A OR
S6A0069X01-C0CX, it accepts the code, but does not change the internal states (RAM and other status of Flags). Busy state, however continues for maximum 40us by the acceptance of the code.

Table 2 The relation between the operation and the combination of RS, R/W

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>E</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
<td>Write instruction code</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td>Read busy flag and address counter</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td>Write data</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td>Read data</td>
</tr>
</tbody>
</table>

When performing data and instruction code by 4 bit, transfer RS, R/W every time.